Features

- **High Performance IDIC® (Extended Read/Write Distance)**
- **Contactless Power Supply**
- **Contactless Read/Write Data Transmission**
- **Radio Frequency f_{RF} from 100 kHz to 150 kHz**
- **Basic Mode or Extended Mode**
- **Compatible with E5551/T5551, T5557, ATA5567**
- **Configurable for ISO/IEC 11784/785 Animal and Waste Standards Compatibility**
- **Total 363 Bits EEPROM Memory: 11 Blocks (32 Bits + 1 Lock Bit)**
- **On Chip Trimmed Capacitor**
- **High Q-antenna Tolerance Due to Build in Options**
- **Adaptable to Different Applications: Access Control, Animal ID and Waste Management**

1. Description

The ATA5577 is a contactless read/write **id**entification **IC** (IDIC) for applications in the 125-kHz or 134-kHz frequency band. A single coil connected to the chip serves as the IC's power supply and bi-directional communication interface. The antenna and chip together form a transponder, or tag.

The on-chip 363-bit EEPROM (11 blocks with 33 bits each) can be read and written block-wise from a base station (reader).

Data is transmitted from the IDIC (uplink) using load modulation. This is achieved by damping the RF field with a resistive load between the two terminals Coil 1 and Coil 2. The IC receives and decodes serial base station commands (downlink) which are encoded as 100% amplitude modulated (OOK) pulse-interval-encoded bit streams.

Full revision datasheet with enhanced data is available on request. Please contact your local sales office.

Read/Write LF RFID IDIC 100 to 150 kHz

ATA5577

Summary

Preliminary

NOTE: This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

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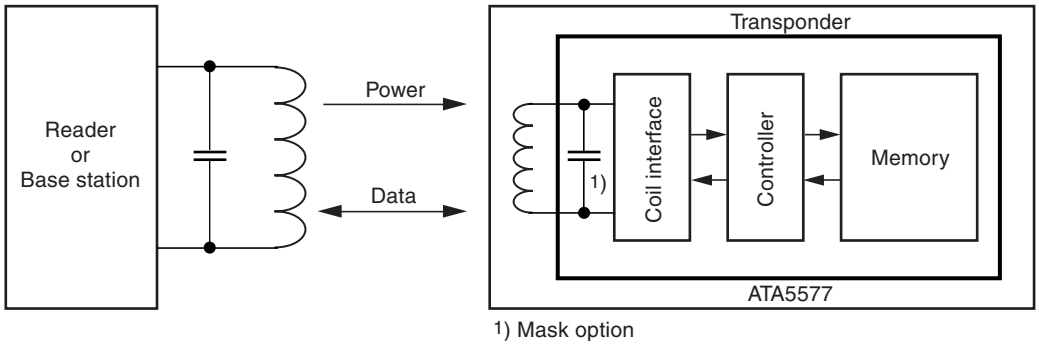
2. Compatibility

The ATA5577 in its *Basic* mode supports the fixed uplink bit rates of the E5551/T5551 transponders. Configuration mapping in Basic mode is compatible to the E5551/T5551. The *Fixed Bit Length* downlink protocol is compatible to the E5551/T5551 and the T5557/ATA5567. This means that the ATA5577 has an easy upgrade path when converting a system from the E5551/T5551 or T5557/ATA5567.

For further details, refer to Atmel®'s Web site for product-relevant application notes.

3. System Block Diagram

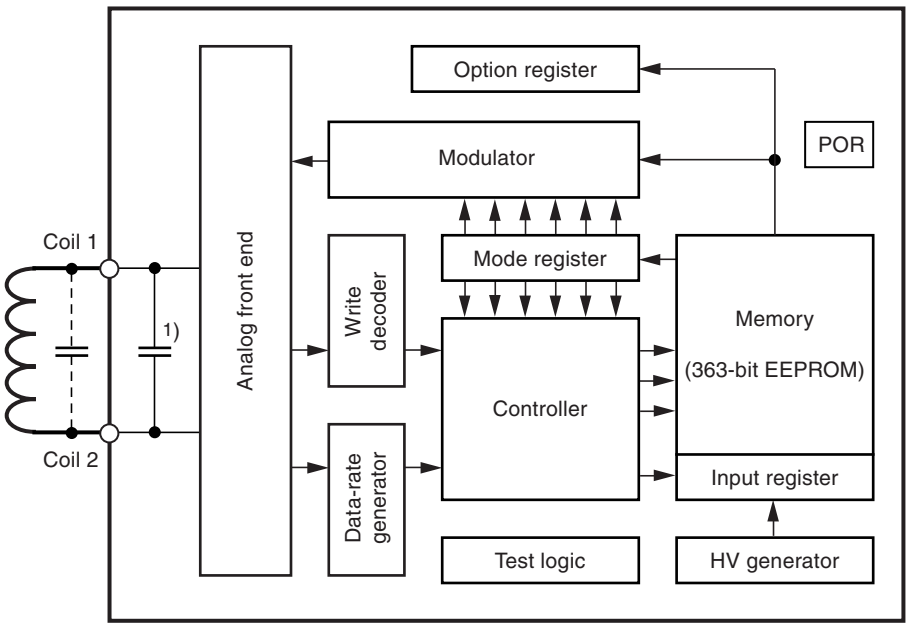
Figure 3-1. RFID System Using ATA5577 Tag



1) Mask option

4. ATA5577 - Functional Blocks

Figure 4-1. Block Diagram



1) Mask option

4.1 Analog Front End (AFE)

The AFE includes all circuits which are directly connected to the coil terminals, generates the IC's power supply, and handles the bi-directional data communication with the reader. It consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- Clock extractor
- Switchable load between Coil 1 and Coil 2 for data transmission from the tag to the reader
- Field-gap detector for data transmission from the base station to the tag
- ESD-protection circuitry

4.2 Data-rate Generator

The data rate is binary programmable to operate at any data rate between RF/2 and RF/128 or to any of the fixed Basic mode data rates (RF/8, RF/16, RF/32, RF/40, RF/50, RF/64, RF/100 and RF/128).

4.3 Write Decoder

The write decoder detects the write gaps and verifies the validity of the data stream according to the Atmel e555x downlink protocol (pulse interval encoding).

4.4 HV Generator

This on-chip charge pump circuit generates the high voltage required to program the EEPROM.

4.5 DC Supply

Power is externally supplied to the IDIC via the two coil connections. The IC rectifies and regulates this RF source and uses it to generate its supply voltage.

4.6 Power-On Reset (POR)

The power-on reset circuit blocks the voltage supply to the IDIC until an acceptable voltage threshold has been reached.

4.7 Clock Extraction

The clock extraction circuit uses the external RF signal as its internal clock source.

4.8 Controller

The control logic module executes the following functions:

- Load mode register with configuration data from EEPROM block 0 after power-on and during reading
- Load option register with the settings for the analog front end stored in EEPROM page 1 block 3 after power-on and during reading
- Control all EEPROM memory read/write access and data protection
- Handle the downlink command decoding, detecting protocol violations and error conditions

4.9 Mode Register

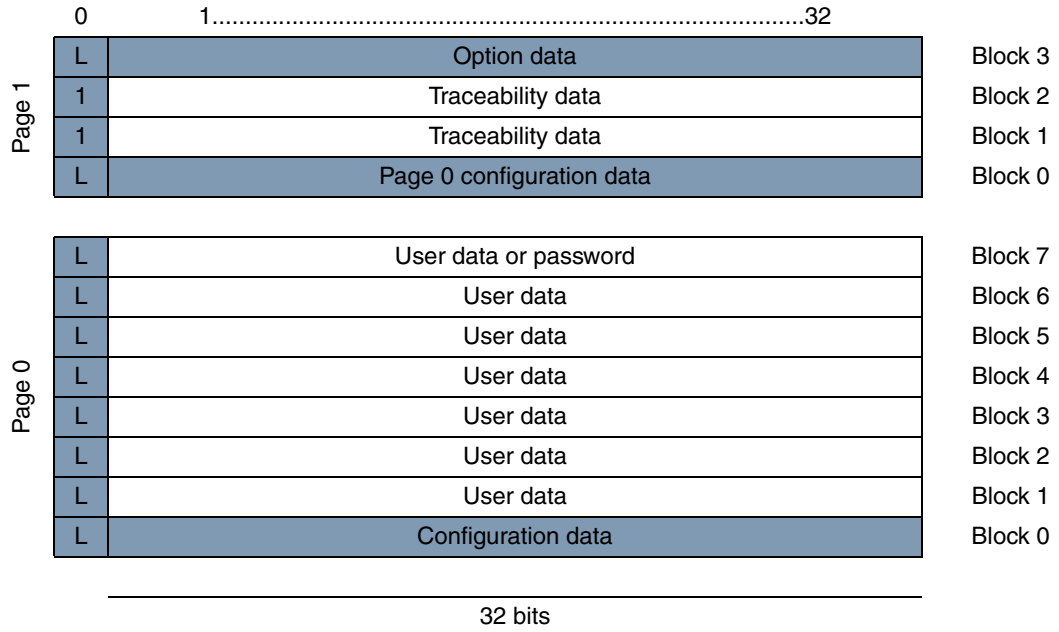
The mode register maintains a readable shadow copy of the configuration data held in block 0 of the EEPROM. It is continually refreshed during read mode and (re-)loaded after every POR event or reset command. On delivery, the mode register is pre-programmed with the value TBD.

4.10 Modulator

The modulator encodes the serialized EEPROM data for transmission to a tag reader or base station. Several types of modulation are available such as: Manchester, bi-phase, FSK, PSK and NRZ.

4.11 Memory

Figure 4-2. Memory Map



The memory is a 363-bit EEPROM, which is arranged in 11 blocks of 33 bits each. Each block includes a single *Lock* bit which is responsible for write-protecting the associated block. Programming takes place on a block basis, so a complete block (including lock bit) can be programmed with a single command. The memory is subdivided into two page areas. Page 0 contains 8 blocks and page 1 contains 4 blocks. All 33 bits of a block, including the lock bit, are programmed simultaneously.

Block 0 of page 0 contains the mode/configuration data, which is not transmitted during regular-read operations. Addressing block 0 will always affect block 0 of page 0 independent of the page selector. Block 7 of page 0 may be used as a write-protection password.

Block 3 of page 1 contains the option register, which is also not transmitted during regular-read operation.

Bit 0 of every block is the lock bit for that block. Once locked, the block (including the lock bit itself) is not re-programmable via the RF field.

Blocks 1 and 2 of page 1 contain traceability data and are transmitted with the modulation parameters defined in the configuration register after the opcode “11” is issued by the reader. These traceability data blocks are programmed and locked by Atmel.

5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Maximum DC current into Coil1/Coil2	I_{coil}	20 (TBD)	mA
Maximum AC current into Coil1/Coil2, f = 125 kHz	$I_{coil\ p}$	20 (TBD)	mA
Power dissipation (die) (free-air condition, time of application: 1s)	P_{tot}	100 (TBD)	mW
Electrostatic discharge maximum to ANSI/ESD-STM5.1-2001 standard (HBM)	V_{max}	2000 (TBD)	V
Operating ambient temperature range	T_{amb}	–40 to +85	°C
Storage temperature range (data retention reduced)	T_{stg}	–40 to +150	°C

6. Electrical Characteristics

T_{amb} = +25°C; f_{coil} = 125 kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
1	RF frequency range		f_{RF}	100	125	150	kHz	
2.1	Supply current (without current consumed by the external LC tank circuit)	T_{amb} = 25°C(1)	I_{DD}		1.5	TBD	mA	T
2.2		Read - full temperature range			2	TBD	mA	Q
2.3		Programming - full temperature range			25	TBD	mA	Q
3.1	Coil voltage (AC supply)	POR threshold (50-mV hysteresis)	$V_{coil\ pp}$	TBD	3.6	TBD	V	Q
3.2		Read mode and write command(2)		6		V_{clamp}	V	Q
3.3		Program EEPROM(2)		8		V_{clamp}	V	Q
4	Start-up time	$V_{coil\ pp}$ = 6V	$t_{startup}$		2.5	TBD	ms	Q
5.1	Clamp voltage (depends on settings in option register)	3-mA current into Coil1/Coil2	$V_{pp\ clamp\ lo}$	TBD	11	TBD	V	Q
5.2			$V_{pp\ clamp\ med}$	TBD	13	TBD	V	Q
5.3			$V_{pp\ clamp\ hi}$	TBD	17	TBD	V	T
5.4		20-mA current into Coil1/Coil2	$V_{pp\ clamp\ med}$	TBD	15	TBD	V	T
6.1	Modulation parameters (depends on settings in option register)	3-mA current into Coil1/Coil2 and modulation ON	$V_{pp\ mod\ lo}$	TBD	3	TBD	V	T
6.2			$V_{pp\ mod\ med}$	TBD	5	TBD	V	Q
6.3			$V_{pp\ mod\ hi}$	TBD	7	TBD	V	Q
6.4		20 mA current into Coil1/Coil2 and modulation ON	$V_{pp\ mod\ med}$	TBD	7.5	TBD	V	T
6.5	Thermal stability		$V_{mod\ lo}/T_{amb}$		–1		mV/°C	Q
7.1	Clock detection level (depends on settings in option register)	$V_{coil\ pp}$ = 8V	$V_{clkdet\ lo}$	TBD	250	TBD	mV	Q
7.2			$V_{clkdet\ med}$	TBD	550	TBD	mV	T
7.3			$V_{clkdet\ hi}$	TBD	800	TBD	mV	Q
7.4	Gap detection level (depends on settings in option register)	$V_{coil\ pp}$ = 8 V	$V_{gapdet\ lo}$	TBD	250	TBD	mV	Q
7.5			$V_{gapdet\ med}$	TBD	550	TBD	mV	T
7.6			$V_{gapdet\ hi}$	TBD	850	TBD	mV	Q
8	Programming time	From last command gap to re-enter read mode (64 + 648 internal clocks)	T_{prog}	5	5.7	6	ms	T
9	Endurance	Erase all/Write all(3)	n_{cycle}	100000			Cycles	Q

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes:
1. I_{DD} measurement set-up R = 100kΩ; $V_{CLK} = V_{coil}$ = 3V: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat. $I_{DD} = (V_{OUTmax} - V_{CLK}) / R$
2. Current into Coil1/Coil2 is limited to 10 mA.
3. Since EEPROM performance is influenced by assembly processes, Atmel confirms the parameters for DOW (tested die on uncut wafer) delivery.

6. Electrical Characteristics (Continued)

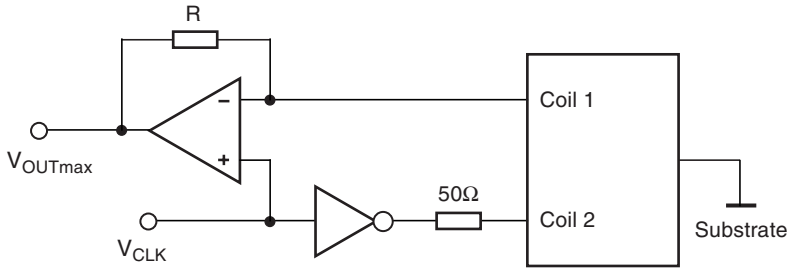
T_{amb} = +25°C; f_{coil} = 125 kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
10.1	Data retention	Top = 55°C(3)	$t_{retention}$	10	20	50	Years	Q
10.2		Top = 150°C(3)	$t_{retention}$	96			hrs	T
10.3		Top = 250°C(3)	$t_{retention}$	24			hrs	Q
11.1	Resonance capacitor	Mask option $V_{coil\ pp}$ = 1V	C_r	320	330	340	pF	T
11.2				242	250	258		
11.3				TBD	130	TBD		
11.4				TBD	75	TBD		
11.5				TBD	10	TBD		Q
12.1	Micromodule capacitor parameters	Capacitance tolerance T_{amb}	C_r	320	330	340	pF	T
12.2		Temperature coefficient	TBD	TBD	TBD	TBD	TBD	TBD

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes:
1. I_{DD} measurement set-up R = 100kΩ; V_{CLK} = V_{coil} = 3V: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat. I_{DD} = (V_{OUTmax} – V_{CLK}) / R
2. Current into Coil1/Coil2 is limited to 10 mA.
3. Since EEPROM performance is influenced by assembly processes, Atmel confirms the parameters for DOW (tested die on uncut wafer) delivery.

Figure 6-1. Measurement Setup for I_{DD}



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-47-50
Fax: (33) 4-76-58-47-60

Literature Requests
www.atmel.com/literature